REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. No amendments to the claims are being made by the present response.

Claims 4, 6, 8, 12, 13, 15, 16, 19, 23-25, 28, 30, 32, 34-36, 39-41, 43, and 45 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,316,818 to Marty, et al. ("Marty, et al.").

It is axiomatic that anticipation under §102 requires the prior art reference disclose every element to which it is applied. *In re King,* 801 F.2d 1324, 1326, 231 USPQ 36, 138 (Fed Cir, 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986). Applicants submit that the pending claims of the present application are not anticipated by the disclosure of Marty, et al.

Applicants' claims include a method for fabricating a bipolar device, recited in Claims 45 and 2–23, and the device therefrom, recited in Claims 24-44. Applicants' claimed method for fabricating a bipolar device includes providing an initial structure including collector 14 and subcollector 12. Next, an n-type region 18 is formed by doping the collector region 14. Following the formation of the n-type dopant region 18, the base region 26 and emitter region 34 are formed. Applicants disclose that the n-type dopant region 18 improves the AC performance of a SiGe heterojunction bipolar transistor as well as the speed and ruggedness of the transistor. Applicants further disclose, referring to Page 3, line 21, that these and other

objects and advantages are achieved in the present invention by a method comprising a low-energy, medium-dose n-type dopant implant after formation of the sub-collector region 12 so as to create a very narrow, medium-dose spike (n-type region) in the low-doped collector region of a high-voltage heterojunction bipolar transistors.

Applicants further disclose that the very narrow n-type region increases performance of applicants' device by delaying the Kirk effect without reducing the breakdown voltage. Referring to Page 7, lines 17-20, of the present application, applicants also disclose that "the inventive n-type region is doped *heavy enough to significantly delay the onset of the Kirk effect, yet narrow enough to avoid creating a high-electric field region of sufficient duration to degrade the breakdown characteristics of the device*". The Kirk effect, a.k.a. base pushout, occurs at high current and is the effective widening of the base region of the device and causes a dramatic increase in the transit time of the carriers in the transistor. The Kirk effect occurs when the current density of carriers through the base collector region exceeds the charge density in the depletion region.

The breakdown voltage is the voltage at which the current within the device increases uncontrollably and the device looses its ability to exhibit switching behavior. Breakdown occurs when additional carriers create an electric field, where the electric field accelerates the charge carriers. As the charge carriers are accelerated, they collide with lattice ions creating additional charge carriers, which may impart ionize additional charge carriers creating an avalanche effect that destroys the switching nature of the device, since the increasing number of charge carriers result in an uncontrollably increasing current.

In conventional semiconductor device processing, there is a tradeoff between the Kirk effect and breakdown voltage. The present invention overcomes the tradeoff between these

properties using a narrow profile n-type dopant region to reduce the Kirk effect without reducing the breakdown voltage. The narrow profile n-type region has a reduced number of charge carriers and therefore does not increase the number of charge carriers to a level that would result in substantial breakdown voltage. Applicants submit that the applied references do not provide a transistor that overcomes the tradeoff between the Kirk effect and breakdown voltage or provide a process that is capable of producing such a transistor.

With respect to applicants' claimed method, the primary reference, Marty, et al., fail to disclose a method of fabricating a bipolar device that includes providing a structure comprising at least a sub-collector region 12, a collector region 14 and isolation regions, said collector region 14 including a deep collector region 16 located therein; forming *an n-type dopant region 14 within a collector region 14 containing a deep collector 16 so as to be in contact with said deep collector 16, said n-type dopant region 18 having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage* and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased, and then *forming a base 26,* as recited in Claim 45.

Marty, et al. provide a method for making a SiGe heterojunction base of a vertical bipolar transistor, which includes providing a Si substrate 1 in which an extrinsic collector buried layer 2 is formed atop the surface of the Si substrate. An epitaxial monocrystalline intrinsic collector 4 is then formed atop the extrinsic collector buried layer 2. Following the formation of short trench isolation regions 5, *three material layers 80, 81, 82, are deposited atop the structure, which later form the base region of the device.* The three material layers include a first layer of undoped Si 80; a second layer of SiGe 81; and an epitaxial layer of P-doped silicon 82. An oxide layer 9 and a nitride layer 10 are then deposited atop the material

layers and etched to form a zone 100. The zone 100 allows for over-doping of the underlying monocrystalline intrinsic collector region 4. *Over-doping the monocrystalline intrinsic collector region 4 of the device by ion implantation forms a selective implantation collector SIC.* Applicants observe that Marty, et al. disclose that the *SIC region is implanted* ***after*** *the formation of the undoped Si layer 80, SiGe layer 81 and boron doped silicon layer 82, of the base stack 8.* Therefore, Marty et al. fail to teach applicants' claimed method comprising forming the n-type doped region first and then later forming the base region 8 of the device, as recited in Claim 45.

Marty, et al. further disclose that the SIC region is formed by implanting through both the SiGe region 81 and base stack 8; see Col. 3, line 66. In order to achieve this result, the prior art process requires a high-energy implant and a light ion, such as phosphorus; see Col. 3, line 66. The resultant implant (SIC) profile produced by the light ion/high-energy implant is a **broad shallow profile**. Subsequent spreading of the highly mobile light ion during high temperature processing steps ensure the formation of a **broad shallow implant profile**, which contacts the base portion of the prior art device. Therefore, Marty, et al. fail to teach a method which includes an *n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage*, as recited in Claim 45.

With respect to applicants' claimed structure, Marty, et al. also fail to teach a bipolar transistor which includes, among other components, an *n-type dopant region that is located atop and in contact with the deep collector and has a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage* and a dopant concentration sufficiently high to restrict base widening when the base-junction is forward biased, as recited in Claim 24. Marty, et al. are defective for failing to teach applicants' claimed structure for the same

reasons as mentioned above. The above statements with respect to an n-type dopant region having *a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage* are therefore incorporated by reference.

It appears to be the Examiner's position that the implant used to form the SIC region in Marty, et al. may be conducted selectively to form applicants' claimed n-type region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage. More specifically, the Examiner refers to Col. 3, lines 65-67, and Col. 4, lines 1-5, of Marty, et al. for the proposition that phosphorous may be deposited "selectively" in a manner which would form applicants' claimed n-type region.

Applicants respectfully disagree and submit that the term "selective" when interpreted in proper context with the complete disclosure of Marty, et al. only denotes that a window 100 formed through the emitter functions as a mask during phosphorus implantation to form the SIC region in an intrinsic base region 4. Marty, et al. fail to disclose containing the high diffusivity phosphorus, implanted during the formation of the broad SIC region, to a vertical width sufficiently narrow to avoid lowering collector base breakdown voltage.

Applicants reiterate that the dopant species, phosphorus, used to form the SIC region is a light ion with a propensity to diffuse through the collector region, especially when implanted with the high implant energies as required of the Marty, et al. process, where the SIC region is formed by implanting phosphorous through three layers of SiGe material. It is well known to those having ordinary skill in the art that the SIC region formed by high energy implantation of phosphorus produces a broad shallow profile that results in a device having performance characteristics consistent with the prior art, as disclosed in the "background of invention section" of applicants' specification. Applicants observe that Marty, et al. discloses

implanting phosphorus to increase the switching speed of the device without providing any instruction for avoiding a reduction in the breakdown voltage. Referring to Col. 4, lines 1-5, the SIC region formed in Marty, et al. is *overdoped* by one or more implant steps in an effort to increase switching speed of the device by implanting more charge carriers. Applicants submit that since Marty, et al. disclose overdoping to increase the switching speed of the device without addressing breakdown voltage, Marty et al. teach away from applicants' present invention including an n-type dopant profile *having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage*, where the narrow vertical width has a *reduced number* of charge carriers yet still decreases the Kirk effect. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Marty, et al. interpreted by one of ordinary skill in the art depicts a semiconducting device in which the speed of the transistor was increased by introducing additional dopant at the expense of a decreasing breakdown voltage.

In summation, applicants respectfully submit that Marty, et al. do not form the SIC region with "selectivity" that could result in an *n-type region having a vertical width sufficiently narrow* to avoid lowering collector-base breakdown voltage, as recited in the applicants' claims. The forgoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention as required by *King* and *Kloster Speedsteel; et. al.*, therefore the claims of the present application are not anticipated by the disclosure of Marty, et al. Applicants respectfully submit that the instant §102 rejection has been obviated and withdrawal thereof is respectfully requested.

Claims 2, 3, 14, 22, 26, 27, and 33, stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. Claims 5 and 29 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. in view of U.S. Patent No. 5,252,841 to Wen, et al. ("Wen, et al."). Claims 7 and 31 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. in view of U.S. Patent No. 5,541,444 to Ohmi, et al. ("Ohmi, et al."). Claims 9, 10, 37, and 38, stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. in view of U.S. Patent No. 3,924,265 to Rogers, et al. ("Rogers, et al."). Claim 11 stands rejected under 35 U.S.C. 103(a) as allegedly obvious over Marty, et al. in view of U.S. Patent No. 6,329,704 to Akatsu, et al. ("Akatsu, et al."). Claims 17 and 42 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. in view of U.S. Patent No. 6,020, 245 to Sato, et al. ("Sato, et al."). Claim 18 stands rejected under 35 U.S.C. §103(a) as allegedly obvious over Marty, et al. in view of Sato, et al. in further view of U.S. Patent No. 6,476, 446 to Ju ("Ju"). Claims 20 and 44 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Marty, et al. in view of U.S. Patent No. 6,429,489 to Botula, et al. ("Botula, et al."). Claim 21 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Marty, et al. in view of U.S. Patent No. 6,410,984 to Trivedi, et al. ("Trivedi, et al.").

Applicants respectfully submit that the claims of the present application are not obvious from any of the applied references cited in the present Office Action since none of the references teaches or suggests applicants' claimed method or structure, recited in Claims 45 and 24, respectively. Specifically, none of the applied references teaches or suggests a method of fabricating a bipolar device which includes a step of *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with the deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid*

lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased, and then a step of *forming a base region*, as recited in Claim 45. Additionally, none of the applied references teaches or suggests a bipolar transistor comprising an *n-type dopant region located atop and in contact with said deep collector and having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage,* as recited in Claim 24. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

The principal reference spurring each of the obviousness rejections, i.e., Marty, et al., is defective for the same reasons as mentioned above. The above statements with respect to Marty, et al. are thus incorporated herein by reference. To reiterate, Marty, et al. fail to teach or suggest a method for producing a bipolar transistor including the step of *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with said deep collector* and then *forming a base*, as recited in Claim 45. Additionally, Marty, et al. fail to teach or suggest the structure produced by applicants' claimed method, as recited in Claim 24.

It is the Examiner's position, that it would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the height of the SiC region in order to adjust the resistance of the collector region.

Applicants respectfully disagree and submit the following: First, since the SIC region is formed by implanting through the overlying base region, 80, 81, 82, a light implant species with a high diffusivity, such as phosphorus, is required. Due to the high diffusivity of the

implant, there is no control of the implant species profile. The resultant profile of a high diffusivity implant is that of a **shallow br ad profile** and not ***a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage,*** as recited in Claim 45. Therefore, it is not within the skill of the art to adjust the height of the SIC region produced by the Marty, et al. method, since the required high diffusivity ion species does not allow such modifications.

Additionally, Marty, et al. teach away from utilizing a heavier low diffusivity implant because a heavier implant, using the Examiners' alleged implant concentration and energy, would destroy the overlying base region 80, 81, 82, therefore degrading the performance of the device to the point of inoperability. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no motivation to make the proposed modification. *In re Gordan*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

With respect to Claims 5 and 29, Wen, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method or structure.

Wen, et al. disclose forming a bipolar transistor where the base-collector capacitance is reduced by eliminating a portion of the collector contact layer 54b underlying the base electrode 66. Wen, et al., referring to FIG. 5, disclose a collector contact 54a formed within a substrate; a collector region 58; a base layer 60; and a emitter 61. The collector region 58, disclosed in *Wen, et al., does not include a deep collector region or an n-type doped region.* Additionally, Wen, et al. fails to teach or suggest a sub-collector region. Therefore, Wen, et al. fail to teach or suggest applicants' claimed method including the steps of *forming an n-*

type dopant region within said collector region so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased, and then *forming a base region,* as recited in Claim 45. Additionally, Wen, et al. fail to teach or suggest applicants' claimed structure including an *n-type dopant region located atop and in contact with said deep collector and having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage*, as recited in Claim 24.

With respect to Claim 7 and 31, Ohmi, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method or structure. Ohmi, et al. disclose in FIG. 1 a device having a substrate 1 including isolation regions 2; an N-type semiconductor buried layer for collector potential 3 positioned atop the substrate 1; a field oxide 4 atop the N-type semiconductor buried layer 3; a base region 7 atop the oxide 4; and an N-type Si layer for forming the emitter region 15. Ohmi, et al. do not teach or suggest forming at least a sub-collector region and a collector region where the collector region includes a deep collector region and an n-type dopant region. Therefore, since Ohmi, et al. fail to disclose forming an n-type doped region, Ohmi, et al. fail to teach or suggest applicants' claimed method.

Additionally, since Ohmi, et al. fail to disclose forming an n-type dopant region, the applied reference also fails to teach or suggest applicants' bipolar transistor comprising an *n-type dopant region located atop and in contact with said deep collector and having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage*, as recited in Claim 24.

With respect to Claims 9, 10, 37 and 38, Rodgers, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method or structure. Rodgers, et al. disclose a V groove MOS transistor having a surface diffused drain and a common substrate source in which a heavily doped base layer and a lightly doped space charge region are provided between the drain and source regions. Rodgers, et al. disclose in FIG. 2 a P-type base region 16 formed over a common source 14, which may be the substrate of the device. A space charge or drift region 18 covers the base region 16. Applicants note that Rodgers, et al. do not make reference to a collector region; therefore Rodgers, et al. do not teach or suggest, forming *a collector region where the collector region includes a deep collector region and an n-type dopant region located therein.* Therefore, since Rodgers, et al. fail to teach or suggest an n-type dopant region within a collector region, Rodgers et al., also fail to teach or suggest a method including *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased*, and then *forming a base region,* as recited in Claim 45.

Rodgers, et al. also fail to teach or suggest applicants' bipolar transistor comprising a *n-type dopant region located atop and in contact with said deep collector and having an vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage,* as recited in Claim 24.

Turning to the rejection of Claim 11, Akatsu, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants'

claimed method, which includes *forming an n-type dopant region within a collector region.* Akatsu, et al. disclose a process and structure that embrace the technique of outdiffusion from an implanted dielectric film. More specifically, Akatsu, et al. disclose a process in which a dielectric film is formed on the silicon substrate and then implanted; where the peak concentration of the implanted dopant species is closer to the silicon substrate/dielectric interface than the upper surface of the dielectric film. The process disclosed in Akatsu, et al. is far removed from applicants' claimed invention. As such, the combination of Marty, et al. and Akatsu, et al. do not teach render applicants' claims obvious.

With respect to Claims 17 and 42, Sato, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method or structure. Sato, et al. disclose a manufacturing method of bipolar transistors allowing omission of photolithographic process of the emitter electrode polysilicon and measurement of the characteristic of the transistor before forming metal electrodes. Sato, et al., referring to Fig. 3(a), disclose a device comprising a P-type silicon substrate 1; N-type buried layer 2 atop the substrate; where a silicon collector region 3_1 is positioned atop the N-type buried layer 2. The collector region 3_1 disclosed in Sato, et al. does not include a deep collector region or an n-type dopant region. Sato, et al. do not teach or suggest *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased,* and then *forming a base region,* as recited in Claim 45.

Since Sato, et al. fail to disclose forming an n-type doped region, Sato, et al. fail to teach or suggest applicants' bipolar transistor comprising an *n-type dopant region located atop and in contact with said deep collector and having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage*, as recited in Claim 24.

With respect to Claim 18, Ju does not alleviate the above defects in Marty, et al. or Sato, et al. since the applied secondary reference does not teach or suggest applicants' claimed method. Ju discloses forming an silicon on insulator (SOI) substrate involving a structure comprising a bulk silicon layer, a buried insulation layer over the bulk silicon layer, a silicon device layer over the bulk silicon layer, a silicon device layer over the buried insulation layer; and a mask layer over the silicon device layer; etching portions of the mask layer, the silicon device layer, and the buried insulation layer thereby forming openings and exposing portions of the bulk silicon layer; depositing polysilicon in the openings; removing a portion of the polysilicon in the openings; removing a portion of the polysilicon in the openings to form polysilicon sidewalls adjacent the silicon device layer and the buried silicon insulation layer and to form gaps at least partially surrounded by the polysilicon sidewalls; depositing an insulation material in the gaps; and removing the mask layer.

Ju is far removed from applicants' claimed method which includes the steps of: *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased*, and then *forming a base region*, as recited in Claim 45.

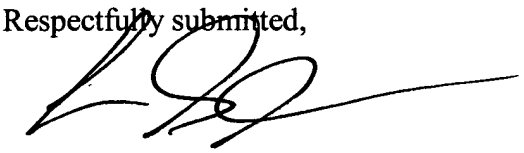
With respect to Claims 22 and 44, Botula, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method or structure. Botula, et al. disclose an ESD device useful in high speed frequency applications where size and loading effects are a concern. More specifically, referring to FIG. 3, a trigger device is disclosed where a SiGe heterojunction bipolar transistor (HBT) is formed on a N-subcollector 302. The SiGe HBT comprises an N-type emitter atop a base region atop an N-collector 308. The collector region 308 disclosed in Botula, et al. does not include a deep collector region or an n-type dopant region. Therefore, Botula, et al. do not teach or suggest applicants' claimed method or structure.

With respect to Claim 21, Trivedi, et al. do not alleviate the above defects in Marty, et al. since the applied secondary reference does not teach or suggest applicants' claimed method. Trivedi, et al. disclose forming an interconnect structure from titanium nitride with tungsten silicide, where the inventive process is suited for use with a gate stack and a contact to an active area in the semiconductor substrate. Trivedi, et al. do not teach or suggest, *forming an n-type dopant region within a collector region containing a deep collector so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased*, and then *forming a base region*, as recited in Claim 45.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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